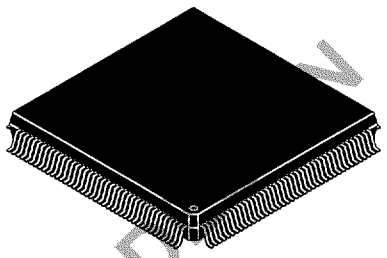
MCD251

Technical Summary

MPEG Full Motion Video Decoder (FMV)



FU SUFFIX
QFP PACKAGE
CASE 1007–01

ORDERING INFORMATION
MCD251FU QFP

This technical summary provides a brief description of the MCD251 MPEG1 Full Motion Video (FMV) Decoder. A complete data sheet for the MCD251 is available and can be ordered from your local Motorola sales office. The order number is MCD251/D.

The MCD251 combines all the functions necessary to implement full motion video decompression with 4 Mbits of DRAM. The device can also be used to display still pictures and brings the possibility of digital full motion imaging technology to cost sensitive computer, communications and consumer applications, e.g. CD–i player full motion video decoder.

Using a combination of Huffman decoding, inverse discrete cosine transform and motion compensation, the MCD251 operates on pixels in 16 x 16 blocks. Each frame of a 352 x 288 pixel, 25 Hz picture sequence is therefore divided into 396 blocks, which are reconstructed in the 4 Mbit DRAM.

The MCD251 is capable of directly driving a 4 Mbit DRAM (256K x 16), including all necessary refresh. The transparent mode allows byte and word accesses by the system bus directly to the DRAM.

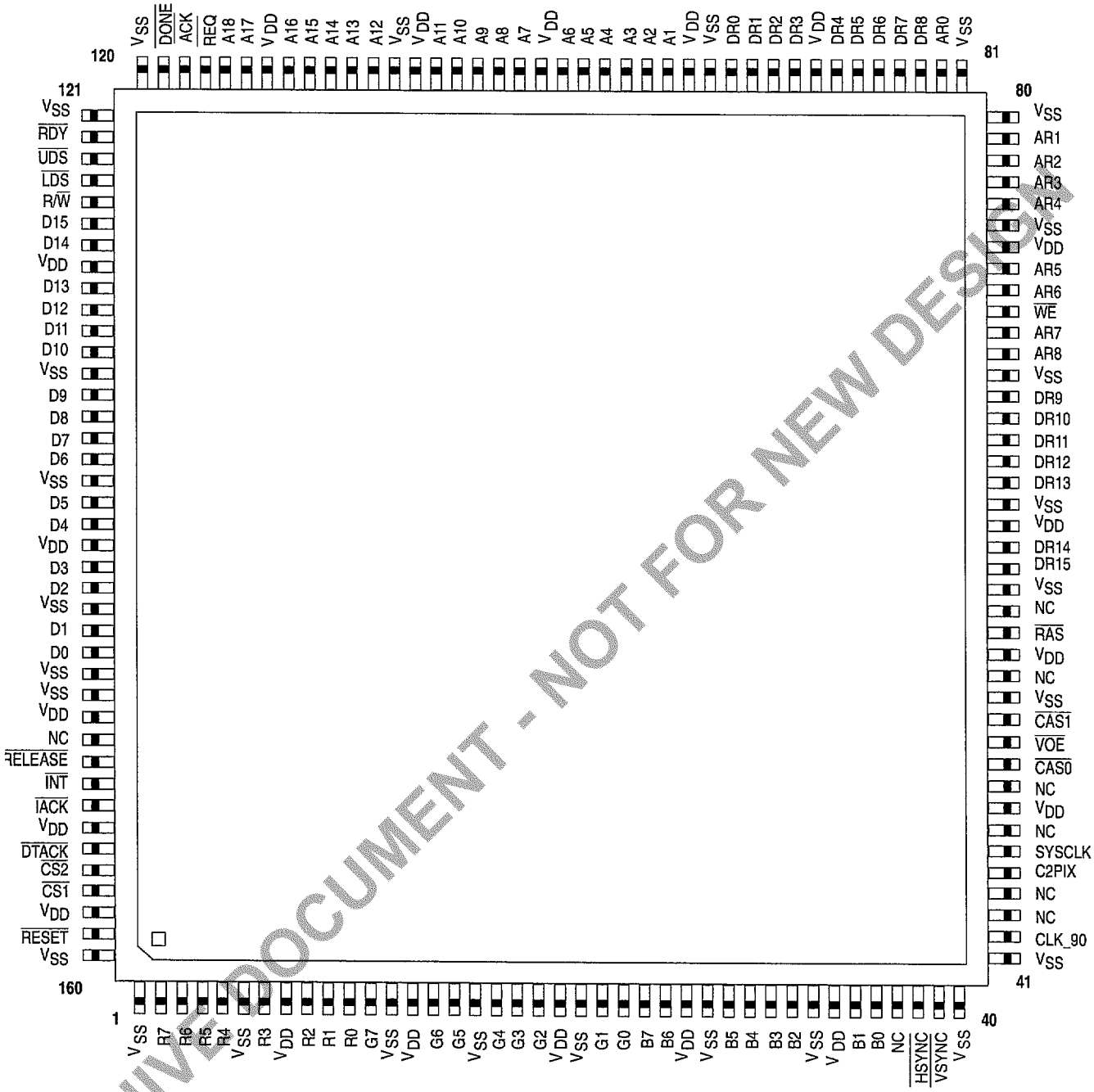
The main features of the MCD251 are as follows:

- Reconstructs Full Motion Video Sequences at 24 Hz, 25 Hz, or 30 Hz and Converts to a 50 Hz or 60 Hz Display Period
- Decodes Data Compatible with the Motion Picture Experts Group (MPEG1) Format at up to 5 Mbit/s
- Outputs the Decoded Video Plus a Border of a Predefined Color as RGB or YUV
- Display is Controlled by Externally Supplied Synchronization Signals and Pixel Clock in Either PAL or NTSC Format
- Able to Decode and Display Still Pictures
- At 30 Hz the Maximum Picture Area is 352 Pixels by 240 Lines
- Maximum Picture Rate of 30 Hz
- 4 Mbit DRAM (256K x 16) Direct Drive via 16 Bidirectional Data Lines and 9 Address Lines
- Compatible with the MC68000 and MC68341 Bus Interfaces
- System Interface that Handles Data Control and Status Information
- Able to Handle a Transfer Rate of up to 10 Mbit/s
- Supports Five Display Modes: Play Forward, Freeze, Single Step Forward, Slow Motion and Scan
- RGB or YUV Output via 24 Data Lines
- CMOS Technology
- 160–Pin Quad Flat Pack (QFP)

NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

PIN ASSIGNMENT



PIN DESCRIPTIONS

Host Interface

Mnemonic	Type	Name and Function
A[18 ... 1]	I	Host address bus.
D[15 ... 0]	B	Host databus. Tri–state. Load 130 pF.
$\overline{CS1}$	I	Chip select 1. Active LOW. For selection of the internal registers. Only A1 ... A12 are significant in this case.
$\overline{CS2}$	I	Chip select 2. Active LOW. For selection of the DRAM. Can only be used when the IC is in transparent or debug mode.
$\overline{UDS}$	I	Upper datastrobe. Active LOW. Indication that data on D8 ... D15 is valid in case of a write cycle to the FMV. In case of a read cycle from the FMV it indicates that the FMV must put data on D8 ... D15.
$\overline{LDS}$	I	Lower datastrobe. Active LOW. Indication that data on D0 ... D7 is valid in case of a write cycle (to the FMV). In case of a read cycle (from the FMV) it indicates that the FMV must put data on D0 .... D7.
$\overline{DTACK}$	B	Active LOW. Data transfer acknowledge output: Indicates in case of a write cycle to the FMV that data is latched. In case of a read cycle from the FMV it indicates that valid data is on the databus. Tri–state, must be pulled up externally. Data transfer acknowledge input: Indicates in case of DMA transfer that there is valid data on the bus. Load 130 pF.
R/$\overline{W}$	I	Read/Write. Indicates the direction of the data flow. High is read from the FMV. Low is write to the FMV.
$\overline{INT}$	O	Interrupt request. Open drain, must be pulled up externally. Active LOW. Load 130 pF.
$\overline{IACK}$	I	Interrupt acknowledge. Active LOW.
$\overline{REQ}$	O	DMA request. Active LOW. Open drain. Must be pulled up externally. Load 130 pF.
$\overline{ACK}$	I	DMA acknowledge. Active LOW.
$\overline{RDY}$	O	DMA ready. Indication that the FMV has latched the data on the bus during a DMA transfer. Tri–state. Must be pulled up externally. Active LOW. Load 130 pF.
$\overline{DONE}$	I	DMA done. Indication that the last DMA transfer is in progress. The FMV will then release the $\overline{REQ}$ signal. Active LOW.
$\overline{RELEASE}$	I	Release DMA request. When asserted the FMV releases $\overline{REQ}$ and resets the internal DMA logic. Active LOW.
CLK_90	I	External 90 kHz clock.
$\overline{RESET}$	I	Global reset. Active LOW.
SYSCLK	I	40 MHz system clock.

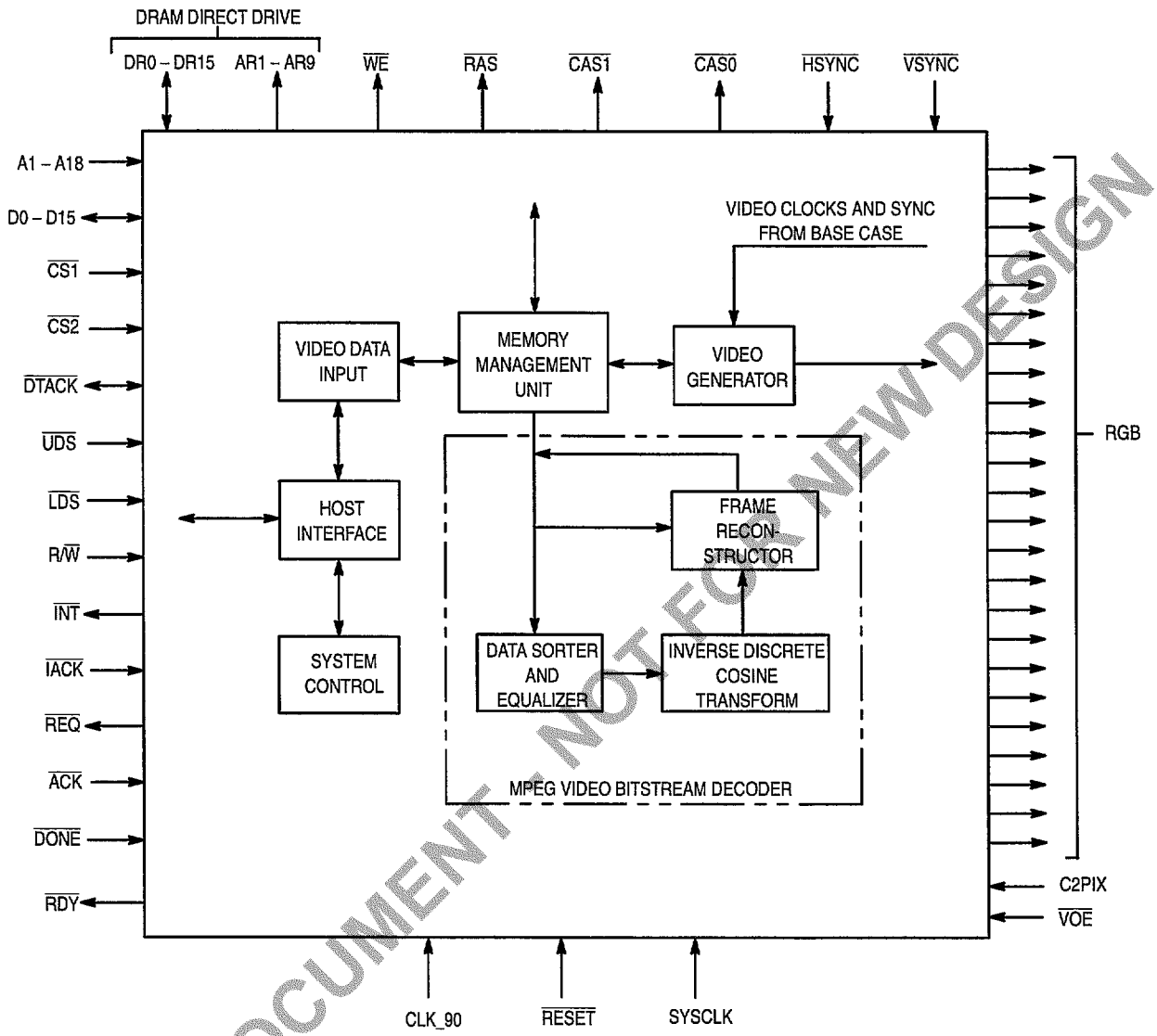
The Video Interface

Mnemonic	Type	Name and Function
R0 ...R7 **G0 ... G7** **B0 ... B7**	O	24 bit RGB bus. When the FMV is in YUV mode, then: R=Y, G=U, B=V. Tri–state. Load 50 pF.
$\overline{VOE}$	I	Video output enable. Enables or tristates the RGB outputs; polarity is defined by a host writeable register bit.
C2PIX	I	Pixel clock of twice the pixel frequency. The clock is internally divided by 2. The phase adjustment is done by the $\overline{HSYNC}$.
$\overline{HSYNC}$	I	Video line synchronization. Active LOW.
$\overline{VSYNC}$	I	Video vertical synchronization signal. Active LOW.

The Memory Interface

Mnemonic	Type	Name and Function
AR0 ... AR8	O	DRAM row / column address. Load 50 pF.
DR0 ... DR15	B	DRAM databus. Tri–state. Load 50 pF.
$\overline{WE}$	O	DRAM write enable. Active LOW. Load 50 pF.
$\overline{RAS}$	O	DRAM row address select. Active LOW. Load 50 pF.
$\overline{CAS0}$	O	Column address select signal for the lower data byte D0 ... D7. Active LOW. Load 50 pF.
$\overline{CAS1}$	O	Column address select signal for the upper data byte D8 ... D15. Active LOW. Load 50 pF.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCD251 Block Diagram should be used in conjunction with the following notes which outline the function of the various blocks within the device:

- The **host interface** takes care of communication with the host processor. It handles data exchange, DMA control and interrupts.
- The **system controller** controls all other functions, reading and interpreting their status and issuing commands.
- The **video data input** pre–processes the incoming data stream. In the case of an ISO11172 (MPEG1) stream, data from the selected channel is extracted from the stream. Also, the complete system layer is removed from the data stream so that data sent to the DRAM consists of MPEG1 video data of the selected channel. The system clock reference data and time stamp data are sent directly to the system controller. The video data input also recognizes the video startcodes and passes them on to the system controller.
- The **memory management unit** handles requests for DRAM access from the video data input, MPEG1 decoder and video generator. It also controls DRAM refresh.
- The **data sorter and dequantizer** takes MPEG1 video data from the FIFO and decodes the variable length codes to produce DCT coefficients, coding type information and motion vectors.
- The **inverse discrete cosine transform** applies a 2–dimensional IDCT on the 8 x 8 coefficient data and passes macroblock data to the frame reconstructor.
- The **frame reconstructor** takes data from the previous or next frame and reconstructs the current frame.
- The **video generator** reads the reconstructed YUV data from one of the buffers, converts it to RGB, fills in the border and outputs the data to a video DAC.

LOGICAL DATA FLOW

The logical data flow between the main elements of the chip is shown in Figure 1.

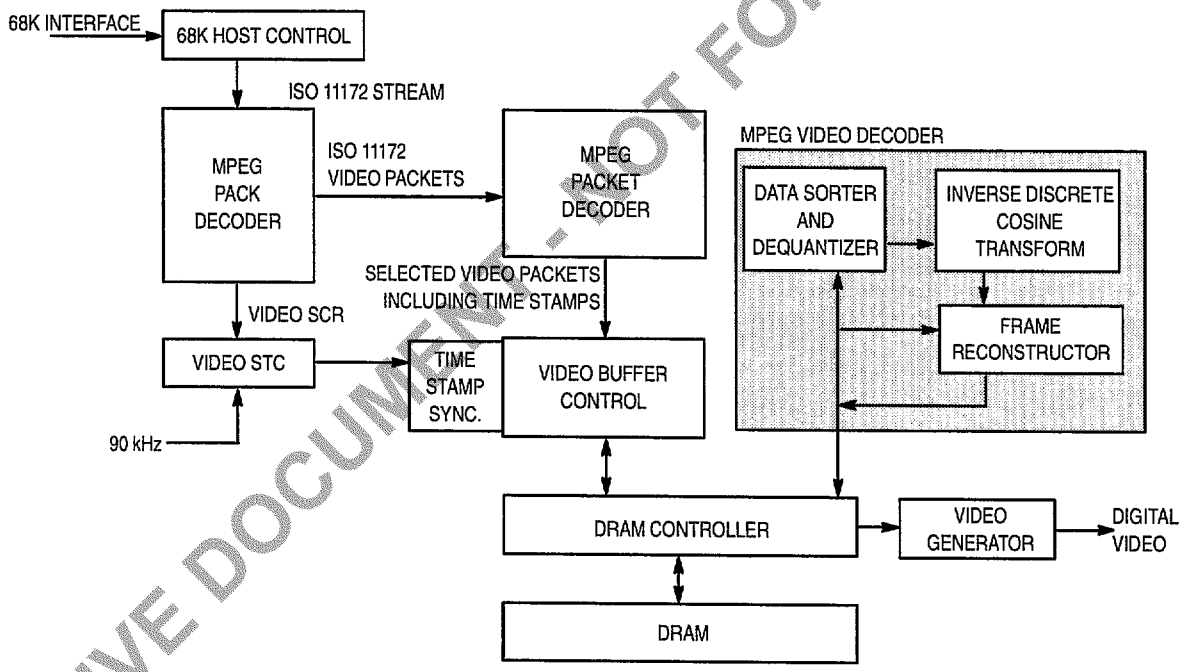


Figure 1. MCD251 Logical Data Flow and Synchronization Diagram

REGISTER MEMORY MAPS

Table 1. Temporal Buffer Registers

Address (HEX)	Register	Description
2	T_PWI	Temporal picture width
4	T_PHE	Temporal picture height
6	T_PRPA	Temporal picture rate/aspect ratio

Table 2. Display Control Buffer_0 Registers

Address (HEX)	Register	Description
1C	B0_TCH	Disp_ctrl_buf_0 time_code_high
1E	B0_TCL	Disp_ctrl_buf_0 time_code_low
20	B0_VSR	Disp_ctrl_buf_0 video status

Table 3. Display Control Buffer_1 Registers

Address (HEX)	Register	Description
30	B1_TCH	Disp_ctrl_buf_1 time_code_high
32	B1_TCL	Disp_ctrl_buf_1 time_code_low
34	B1_VSR	Disp_ctrl_buf_1 video status

Table 4. Display Control Buffer_2 Registers

Address (HEX)	Register	Description
44	B2_TCH	Disp_ctrl_buf_2 time_code_high
46	B2_TCL	Disp_ctrl_buf_2 time_code_low
48	B2_VSR	Disp_ctrl_buf_2 video status

Table 5. Video Control Registers

Address (HEX)	Register	Description
66	Br	Border_red register
68	Bg	Border_green register
6A	Bb	Border_blue register
6C	Yo	Y–offset register
6E	Xo	X–offset register
70	Ya	Y–active register
72	Xa	X–active register
74	Yd	Y–display register
76	Xd	X–display register
78	Wh	Window height register
7A	Ww	Window width register
7C	Yw	Y–window register
7E	Xw	X–window register

Table 6. System Control Registers

Address (HEX)	Register	Description
50	SYS_STAT	Decoder status
52	SYS_PWI	Picture width
54	SYS_PHE	Picture height
56	SYS_PRPA	Picture rate/aspect ratio
58	SYS_TCH	Time code high
5A	SYS_TCL	Time code low
5C	SYS_VSR	Video status
5E	SYS_STS	System status
60	SYS_IER	Interrupt enable
62	SYS_ISR	Interrupt status
64	SYS_TIM	Timer
C0	SYS_SCMD	System command
C2	SYS_VCMD	Video command
C4	SYS_STRsel	Stream select
C6	SYS_SCR	System control
DA	SYS_GCR	Global control
DC	SYS_ICR	Interrupt control
DE	SYS_VDI	Video data input
E4	SYS_ABS	Actual buffer size
F2	SYS_BSIZ	Block size

Table 7. MMU Registers

Address (HEX)	Register	Description
F4	MMU_FSTART	FIFO start pointer

Table 8. Microcode RAM

Address (HEX)	Description
800	Bank1 bit 16 – 25, bit 35 – 40
1000	Bank2 bit 0 – 15
1800	Bank3 bit 26 – 34

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) ..... 0°C to 70°C
Voltage, V_{DD} ..... 5 V ± 10%
Voltage, V_{SS} ..... 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 7.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage	– 0.5 to V_{DD} + 0.5	V
I	DC Current Drain, per Pin	25	mA
I	DC Current Drain, V_{DD}/V_{SS} Pins	75	mA
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (10 Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

FMV/CD–i ARCHITECTURE

In a CD–i player as shown in Figure 2, FMV provides the complete functionality of the full motion video extensions as specified in the Green Book standard for CD–i. It requires the external 4 Mbit DRAM to support MPEG video decoding, but can use the video DACs which are already part of the base case CD–i architecture. Video decoding is synchronized to the base case video decoder, (MCD211, VDSC) and its video output is multiplexed with VDSC output on a pixel by pixel basis.

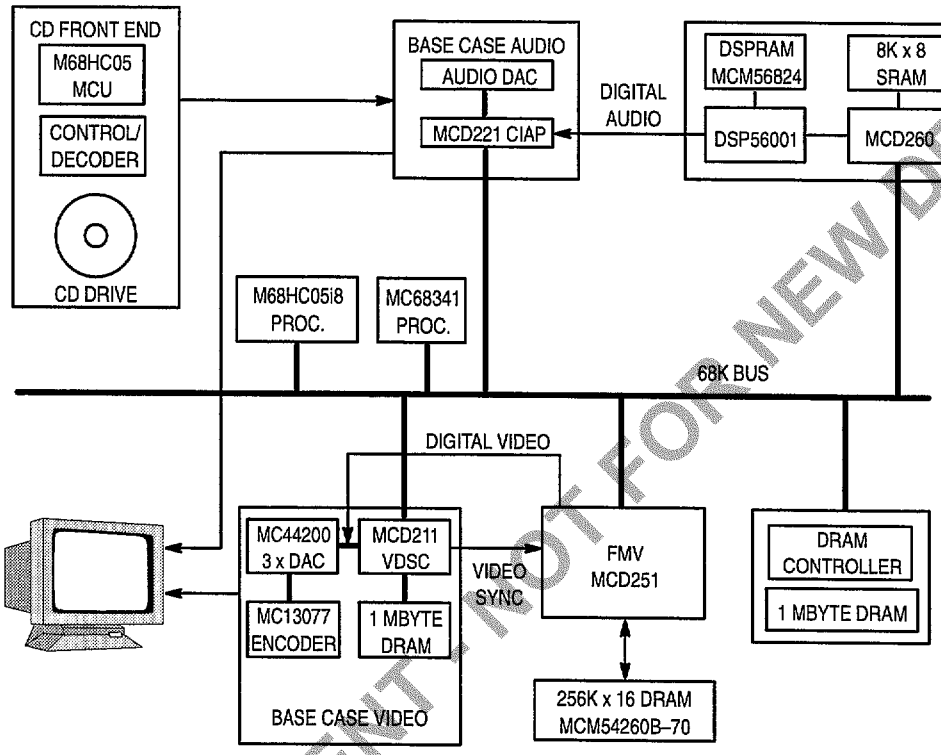


Figure 2. FMV/CD–i Architecture

DIGITAL VIDEO SWITCHING BETWEEN VDSC AND FMV

Digital or analog multiplexing may be used with FMV. Figure 3 shows how only one video DAC may be used if digital multiplexing is implemented. Digital video is tied directly to the 24 bit RGB bus from the base case video decoder (MCD211, VDSC) and multiplexing is achieved by a switch signal from VDSC, which enables and disables pixel outputs from the two sources.

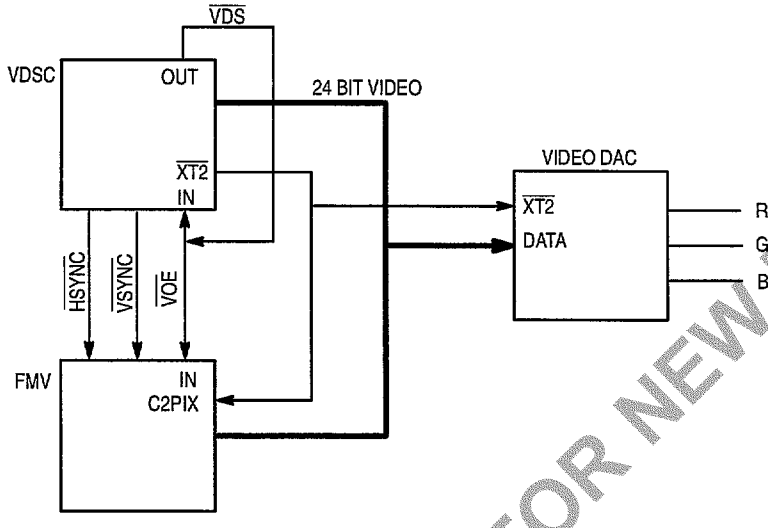


Figure 3. Digital Video Switching Example

ANALOG VIDEO SWITCHING BETWEEN VDSC AND FMV

Figure 4 shows a configuration more suited to an approach in which MPEG1 is added to a basic CD–i player as an expansion cartridge. FMV video decoding is still synchronized to the relevant base case signals, but the multiplexing and mixing are done in the analog domain. Although this requires two DACs, it requires fewer pins on the expansion cartridge connector.

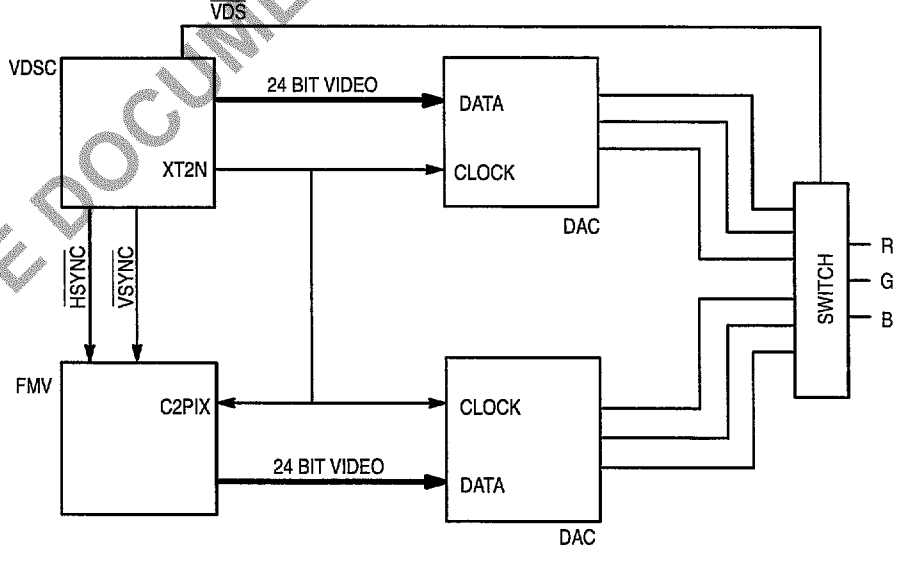


Figure 4. Analog Video Switching Example

FMV IN A PC MULTIMEDIA APPLICATION

Figure 5 illustrates how FMV could be used in a PC based application to provide an MPEG playback window overlayed on a VGA display. The VGA overlay controller provides scan rate conversion of the decoded MPEG image and windowing control based on color keying or programmable XY coordinates. An analog video switch is controlled from this to provide the overlay function.

Using FMV in this standalone manner requires the addition of a TV sync generator to provide $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and a pixel clock to FMV.

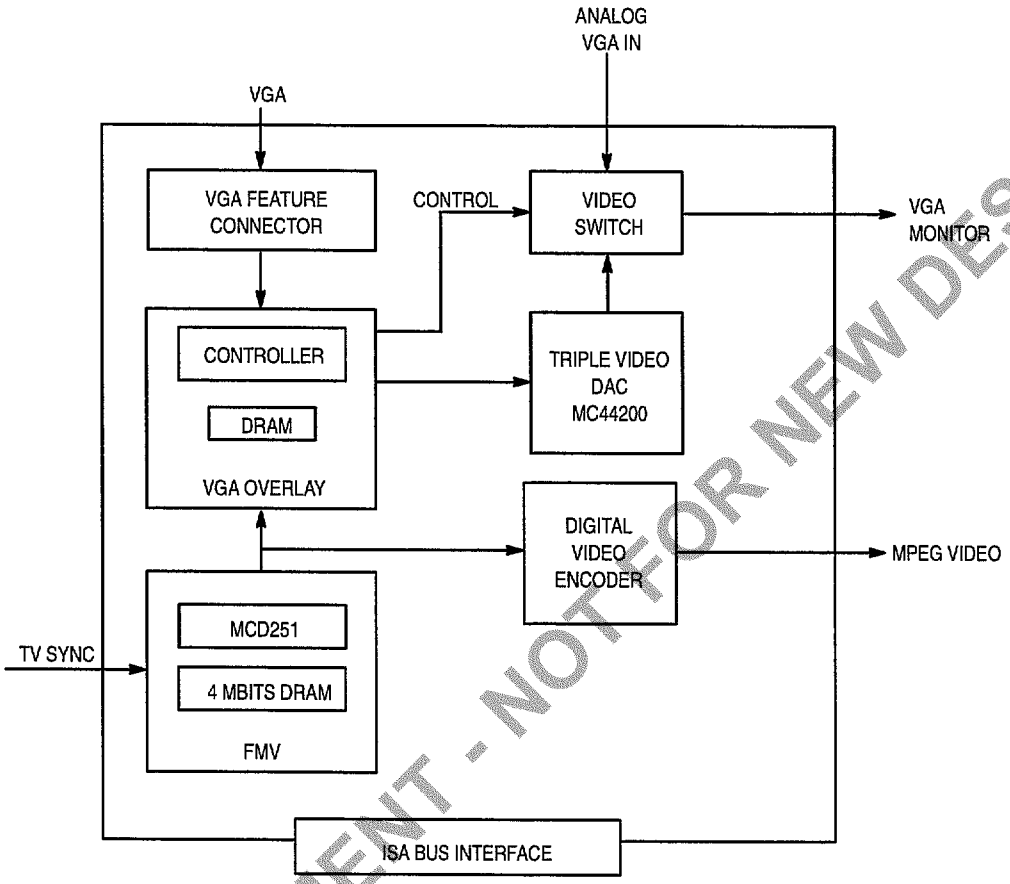


Figure 5. Example of FMV in a PC Multimedia Application

VIDEO ON DEMAND

FMV may be used as the decoder section of a video on demand integrated receiver decoder, as illustrated in Figure 6. MPEG1 video and audio streams are carried over an asymmetric digital subscriber loop (ADSL) in an MPEG2 transport stream. A transport stream decoder separates the conditional access data and the video and audio streams from the transport stream. The video stream is directed to FMV and the conditional access data to the Smart Card controller. An on–screen display is generated by using an MCD211 (VDSC). The video output stage is identical to those in the CD–i application described earlier.

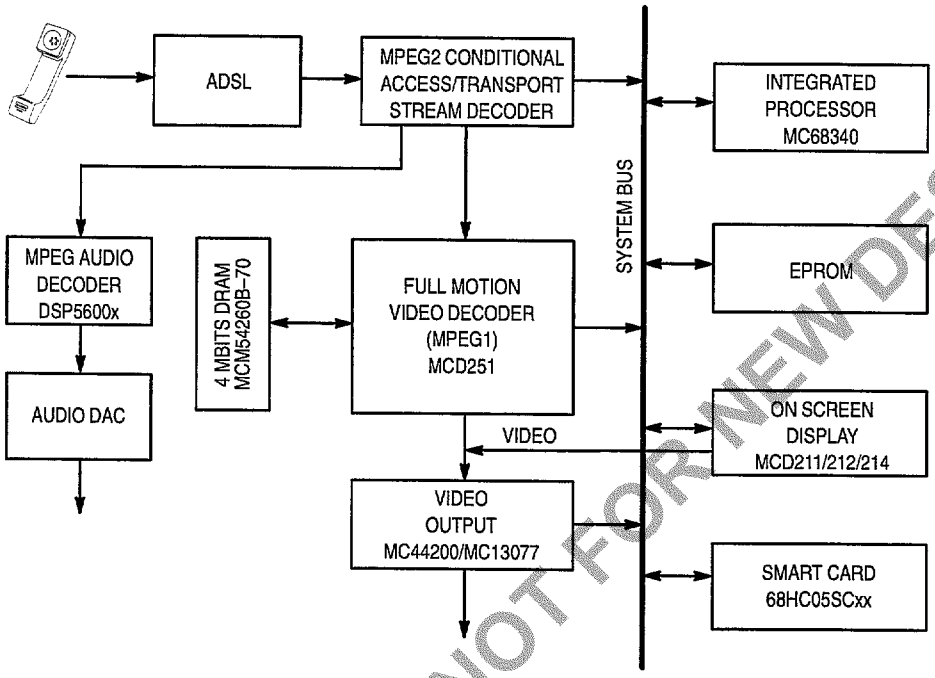


Figure 6. Example of Video On Demand

PACKAGE DIMENSIONS

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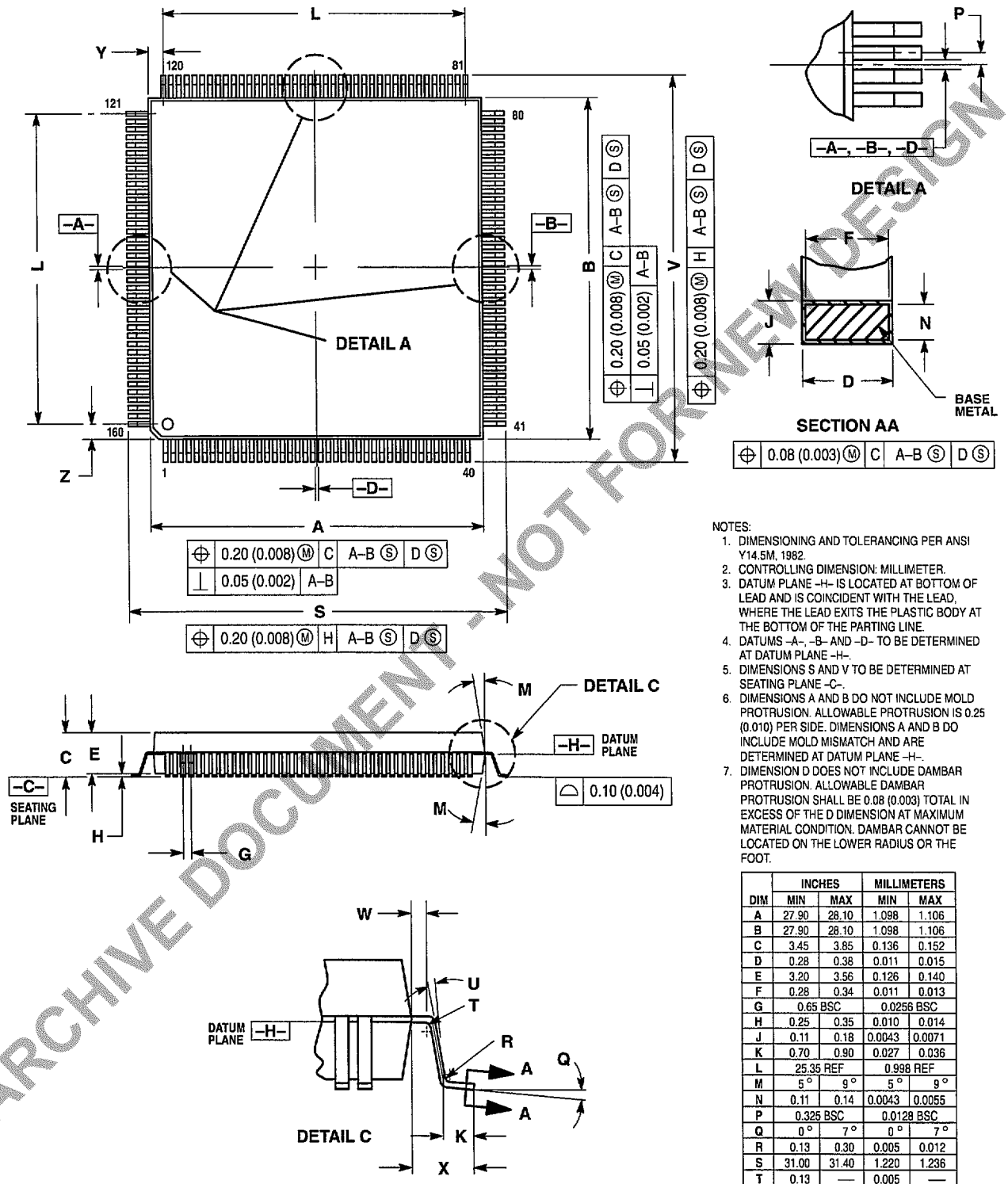

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD, WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	3.85	0.136	0.152
D	0.28	0.38	0.011	0.015
E	3.20	3.56	0.126	0.140
F	0.28	0.34	0.011	0.013
G	0.65 BSC		0.0256 BSC	
H	0.25	0.35	0.010	0.014
J	0.11	0.18	0.0043	0.0071
K	0.70	0.90	0.027	0.036
L	25.35 REF		0.998 REF	
M	5°	9°	5°	9°
N	0.11	0.14	0.0043	0.0055
P	0.325 BSC		0.0128 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.325 REF		0.0522 REF	
Z	1.325 REF		0.0522 REF	

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